

Figures

Figure 1: A line graph showing the relationship between the number of hours spent studying and the score on a test. The x-axis represents hours (0 to 10) and the y-axis represents score (0 to 100). The data points are (0, 0), (1, 10), (2, 20), (3, 30), (4, 40), (5, 50), (6, 60), (7, 70), (8, 80), (9, 90), and (10, 100). The line is a straight line passing through the origin.

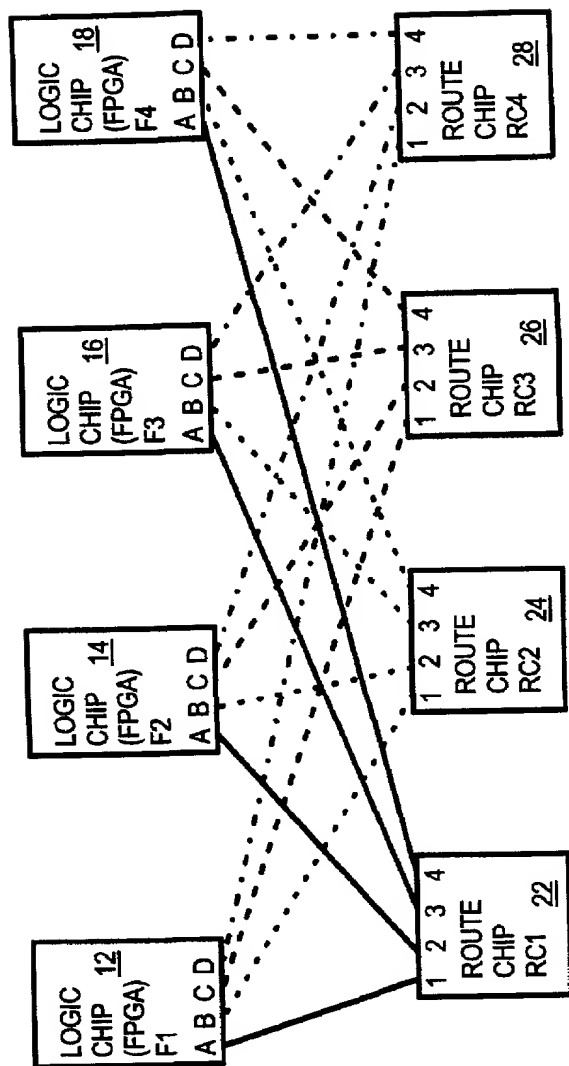


FIG. 1

PRIOR ART

FIG. 2

PRIOR ART

	PIN A	PIN B	PIN C	PIN D
FPGA - F1	RC1	RC2	RC3	RC4
FPGA - F2	RC1	RC2	RC3	RC4
FPGA - F3	RC1	RC2	RC3	RC4
FPGA - F4	RC1	RC2	RC3	RC4

FIG. 3

PRIOR ART

	PIN A	PIN B	PIN C	PIN D
FPGA - F1		X2-RC2	X3-RC3	
FPGA - F2	X1-RC1			X4-RC4
FPGA - F3	X1-RC1	X2-RC2	X3-RC3	X4-RC4
FPGA - F4				

X5 X6

X5 X6

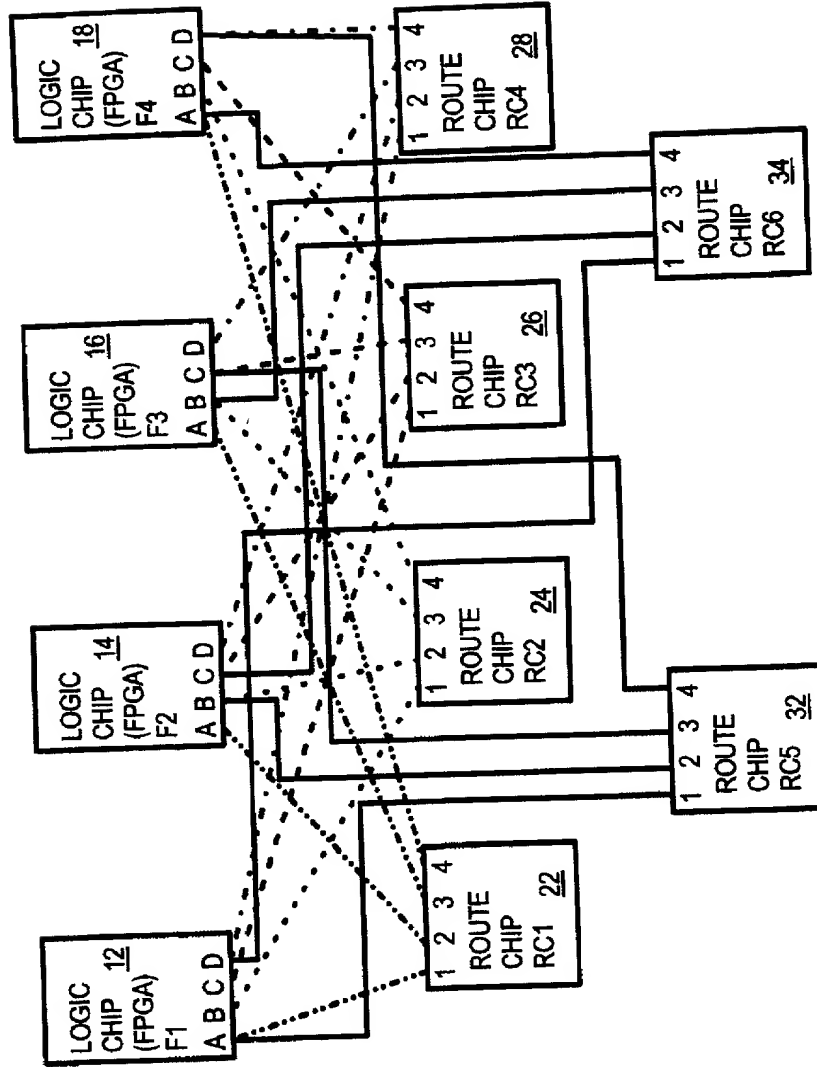


FIG. 4

	PIN A	PIN B	PIN C	PIN D
FPGA - F1	RC1	RC2	RC3	RC4
FPGA - F2	RC1	RC2	RC3	RC4
FPGA - F3	RC1	RC2	RC3	RC4
FPGA - F4	RC1	RC2	RC3	RC4

FIG. 5A

FIG. 5B

	PIN A	PIN B	PIN C	PIN D
FPGA - F1	X5	X2-RC2	X3-RC3	X6
FPGA - F2	X1-RC1	X5	X6	X4-RC4
FPGA - F3	X1-RC1	X2-RC2	X3-RC3	X4-RC4
FPGA - F4				

FIG. 6

FIG. 7

	PIN A	PIN B	PIN C	PIN D
FPGA - F1	X1	X2	X5	X4
FPGA - F2	X1		X5	X6
FPGA - F3	X3	X2		X6
FPGA - F4	X3			X4

X1: F1-F2
X2: F1-F3
X3: F3-F4
X4: F1-F4
X5: F1-F2
X6: F2-F3
X7: F2-F3

PRIOR ART

FIG. 8

	PIN A	PIN B	PIN C	PIN D
FPGA - F1	X1	X2	X5	X4
FPGA - F2	X1	X7	X5	X6
FPGA - F3	X3	X2	X7	X6
FPGA - F4	X3			X4

X1: F2-F3
 X2: F2-F3
 X3: F1-F2
 X4: F1-F3
 X5: F3-F4
 X6: F1-F4
 X7: F1-F2

	PIN A	PIN B	PIN C	PIN D
FPGA - F1		X4	X3	X6
FPGA - F2	X2		X3	X1
FPGA - F3	X2	X4	X5	X1
FPGA - F4			X5	X6

FIG. 9

PRIOR ART

	PIN A	PIN B	PIN C	PIN D
FPGA - F1	X7	X4	X3	X6
FPGA - F2	X2	X7	X3	X1
FPGA - F3	X2	X4	X5	X1
FPGA - F4			X5	X6

FIG. 10

ORIGINAL

X1: F1-F3
X2: F1-F4
X3: F2-F3
X4: F3-F4
X5: F2-F3
X6: F1-F4

SHUFFLED

X1: F1-F3
X2: F1-F4
X3: F1-F3
X4: F2-F3
X5: F3-F4
X6: F1-F4

	PIN A	PIN B	PIN C	PIN D
FPGA - F1		X2	X1	X3
FPGA - F2		X4		
FPGA - F3	X5	X4	X1	X3
FPGA - F4	X5	X2		

FIG. 11

PRIOR ART

	PIN A	PIN B	PIN C	PIN D
FPGA - F1	X6	X2	X1	X3
FPGA - F2		X4		
FPGA - F3	X5	X4	X1	X3
FPGA - F4	X5	X2		X6

FIG. 12

X1: F4-F5
 X2: F4-F5
 X3: F2-F5
 X4: F4-F5
 X5: F4-F5
 X6: F2-F5
 X7: F2-F5
 X8: F2-F5
 X9: F2-F4
 X10: F2-F4
 X11: F2-F4
 X12: F2-F4

FIG. 13

PRIOR ART

	A	B	C	D	E	F	G	H
FPGA - F1								
FPGA - F2					X3	X6	X7	X8
FPGA - F3								
FPGA - F4	X1	X2	X5	X4				
FPGA - F5	X1	X2	X5	X4	X3	X6	X7	X8
FPGA - F6								
FPGA - F7								
FPGA - F8								

X9,10,11,12

X9,10,11,12

X1: F4-F5
X2: F4-F5
X3: F2-F5
X4: F4-F5
X5: F4-F5
X6: F2-F5
X7: F2-F5
X8: F2-F5
X9: F2-F4
X10: F2-F4
X11: F2-F4
X12: F2-F4

FIG. 14

	A	B	C	D	E	F	G	H
FPGA - F1								
FPGA - F2	X7	X9	X10	X3	X6	X11	X12	X8
FPGA - F3								
FPGA - F4	X10	X2	X4	X9	X12	X5	X1	X11
FPGA - F5	X7	X2	X4	X3	X6	X5	X1	X8
FPGA - F6								
FPGA - F7								
FPGA - F8								

FIG. 15

	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	R15	R16
	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P
FPGA - F1	R17			R18	R19			R20	R21			R22	R23			R24
FPGA - F2																
FPGA - F3																
FPGA - F4	R18			R17	R20			R19	R22			R21	R24			R23
FPGA - F5	R17			R18	R19			R20	R21			R22	R23			R24
FPGA - F6																
FPGA - F7																
FPGA - F8	R18			R17	R20			R19	R22			R21	R24			R23
FPGA - F9	R17			R18	R19			R20	R21			R22	R23			R24
FPGA - F10																
FPGA - F11																
FPGA - F12	R18			R17	R20			R19	R22			R21	R24			R23
FPGA - F13	R17			R18	R19			R20	R21			R22	R23			R24
FPGA - F14																
FPGA - F15																
FPGA - F16	R18			R17	R20			R19	R22			R21	R24			R23